CLAIMS:

1. A method of forming a semiconductor memory device comprising:

forming a plurality of openings over a substrate;

forming second sidewall spacers comprising a first dielectric material within each of the openings;

narrowing the openings by covering interiors of the second sidewall spacers with a second dielectric material that is different from the first dielectric material;

filling the openings with conductive material to form a contact in electrical communication with a node on the substrate;

selectively removing substrate material to define a first set of containers having first container sidewalls;

forming first sidewall spacers adjacent the first container sidewalls; and

selectively removing remaining substrate material adjacent the first sidewall spacers to define a second set of containers.

2. The method of claim 1, further comprising forming capacitors in the containers separated only by the spacers.

3. The method of claim 1, further comprising:

forming a first capacitor plate in each of the first and second containers, the first capacitor plate comprising hemispherical polysilicon in electrical communication with a respective node within respective containers of the first and second containers, respective first capacitor plates being insulated from one another by the first sidewall spacers;

forming a dielectric layer covering each respective first capacitor plate; and

forming a second capacitor plate on the dielectric layer.

4. The method of claim 1, wherein filling the openings with conductive material comprises filling the openings with conductive polysilicon.

5. The method of claim 1, wherein forming second sidewall spacers within each of the openings comprises:

depositing a dielectric layer comprising silicon nitride to form the first dielectric material; and

anisotropically etching the dielectric layer to expose the node.

6. The method of claim 1, wherein narrowing the openings comprises:

depositing a layer of the second dielectric material comprising silicon dioxide; and

anisotropically etching the layer of second dielectric material to expose the node.

7. The method of claim 1, wherein selectively removing substrate material to define a first set of containers having first container sidewalls comprises:

plasma etching the substrate material to form a first set of containers;

forming a dielectric layer in the first set of containers; and

anisotropically etching the dielectric layer to form sidewalls in the first set of containers.

8. The method of claim 1, wherein selectively removing remaining substrate material adjacent the spacers to define a second set of containers comprises wet etching the remaining substrate material selectively with respect to the first and second sidewall spacers.

9. The method of claim 1, wherein forming an opening comprises forming a bit line contact opening.

10. A method of forming a semiconductor memory device comprising:

forming a plurality of openings over a substrate, individual openings having at least one sidewall;

covering the at least one sidewall of the plurality of openings with a first insulating material;

etching the first insulating material to form second sidewall spacers;

narrowing the openings by covering interiors of the second sidewall spacers with a second insulating material that is different from the first insulating material;

forming electrically conductive material in the openings to provide contacts;

selectively removing substrate material to define a first set of containers having container sidewalls, wherein defining the first set of containers includes selectively etching the first set of containers relative to the sidewall spacers and the electrically conductive material of the contacts;

forming first sidewall spacers adjacent the container sidewalls; and

selectively removing remaining substrate material adjacent the first sidewall spacers to define a second set of containers.

11. The method of claim 10, further comprising forming capacitors in the containers separated only by the spacers.

12. The method of claim 10, further comprising:

forming a first capacitor plate in each of the first and second containers, the first capacitor plate comprising hemispherical polysilicon in electrical communication with a respective node within respective containers of the first and second containers, respective first capacitor plates being insulated from one another by the first sidewall spacers;

forming a dielectric layer covering each respective first capacitor plate; and

forming a second capacitor plate on the dielectric layer.

13. The method of claim 10, wherein forming electrically conductive material in the openings comprises filling the openings with conductive polysilicon.

14. The method of claim 10, wherein forming second sidewall spacers within each of the openings comprises:

depositing a dielectric layer comprising silicon nitride to form the first insulating material; and

anisotropically etching the dielectric layer to expose the node.

15. The method of claim 10, wherein narrowing the openings comprises:

depositing a layer of the second insulating material comprising silicon dioxide; and

anisotropically etching the layer of second insulating material to expose the node.

16. The method of claim 10, wherein selectively removing substrate material to define a first set of containers having first container sidewalls comprises:

plasma etching the substrate material to form a first set of containers;

forming a dielectric layer in the first set of containers; and

anisotropically etching the dielectric layer to form sidewalls in the first set of containers.

17. The method of claim 10, wherein selectively removing remaining substrate material adjacent the spacers to define a second set of containers comprises wet etching the remaining substrate material selectively with respect to the first and second sidewall spacers.

18. The method of claim 10, wherein forming a plurality of openings over a substrate includes forming a plurality of bit line contact openings over a substrate.

19. A method of forming a contact comprising:

forming a sacrificial layer over a node on a substrate;

forming an opening through the sacrificial layer and extending to the node;

forming a first dielectric sidewall coating an interior sidewall of the opening;

forming a second dielectric sidewall coating an interior sidewall of the first dielectric sidewall; and

forming a conductive plug within an interior sidewall of the second dielectric layer and extending through the opening to the node.

20. The method of claim 19, wherein forming a first dielectric sidewall comprises:

depositing a layer of first dielectric material comprising silicon nitride; and

anisotropically etching the layer of first dielectric material to expose the node.

21. The method of claim 19, wherein forming a second dielectric sidewall comprises:

depositing a layer of second dielectric material comprising silicon dioxide; and

anisotropically etching the layer of second dielectric material to expose the node.

22. The method of claim 19, wherein forming a conductive plug comprises forming a plug of conductive polysilicon in electrical communication with the node.

23. The method of claim 19, wherein forming a second dielectric sidewall comprises forming a second dielectric sidewall that is thicker than a thickness of the first dielectric sidewall.

24. The method of claim 19, wherein forming a second dielectric sidewall comprises forming a second dielectric sidewall that has a relative dielectric constant that is less than a relative dielectric constant of the first dielectric sidewall.

25. A method of forming a semiconductor memory device comprising:

forming a plurality of openings over a substrate;

forming second sidewall spacers comprising a first dielectric material within each of the openings;

filling the openings with conductive material to form a contact in electrical communication with a node on the substrate;

forming a negative photoresist mask to define a first set of openings;

etching substrate material through the first set of openings to define a first set of containers having first container sidewalls;

forming first sidewall spacers adjacent the first container sidewalls; and

selectively removing remaining substrate material adjacent the first sidewall spacers to define a second set of containers.

26. The method of claim 25, further comprising:

narrowing the openings by covering interiors of the second sidewall spacers with a second dielectric material that is different from the first dielectric material prior to filling the openings; and

forming capacitors in the containers separated only by the spacers.

27. The method of claim 25, further comprising:

forming a first capacitor plate in each of the first and second containers, the first capacitor plate comprising hemispherical polysilicon in electrical communication with a respective node within respective containers of the first and second containers, respective first capacitor plates being insulated from one another by the first sidewall spacers;

forming a dielectric layer covering each respective first capacitor plate; and

forming a second capacitor plate on the dielectric layer.

28. The method of claim 25, wherein filling the openings with conductive material comprises filling the openings with conductive polysilicon.

29. The method of claim 25, wherein forming second sidewall spacers within each of the openings comprises:

depositing a dielectric layer comprising silicon nitride to form the first dielectric material; and

anisotropically etching the dielectric layer to expose the node.

30. The method of claim 25, wherein narrowing the openings comprises:

depositing a layer of the second dielectric material comprising silicon dioxide; and

anisotropically etching the layer of second dielectric material to expose the node.

31. The method of claim 25, wherein selectively removing substrate material to define a first set of containers having first container sidewalls comprises:

plasma etching the substrate material to form a first set of containers;

forming a dielectric layer in the first set of containers; and

anisotropically etching the dielectric layer to form sidewalls in the first set of containers.

32. The method of claim 25, wherein selectively removing remaining substrate material adjacent the spacers to define a second set of containers comprises wet etching the remaining substrate material selectively with respect to the first and second sidewall spacers.

33. The method of claim 25, wherein forming an opening comprises forming a bit line contact opening.

34. A bit line contact comprising:

a layer formed on a substrate and including an opening extending through the layer to a node on the substrate;

a first dielectric sidewall formed in the opening and coating an interior sidewall of the opening;

a second dielectric sidewall formed in the opening and coating an interior sidewall of the first dielectric layer; and

a conductive plug formed within an interior sidewall of the second dielectric layer and extending through the opening to the node.

35. The bit line contact of claim 34, wherein the first dielectric sidewall is formed of a first material and the second dielectric sidewall is formed of a second material having a lower relative dielectric constant than the first dielectric sidewall.

36. The bit line contact of claim 34, wherein the conductive plug comprises doped polysilicon.

37. The bit line contact of claim 34, wherein the contact is laterally surrounded by six capacitors.

38. The bit line contact of claim 34, wherein the first dielectric sidewall has an aspect ratio of twenty five or more.

39. The bit line contact of claim 34, wherein the first dielectric sidewall comprises silicon nitride.

40. The bit line contact of claim 34, wherein the second dielectric sidewall comprises silicon dioxide.

41. The bit line contact of claim 34, wherein the second dielectric sidewall is thicker than the first dielectric sidewall.